ABSTRACT OF THE DISCLOSURE

Disclosed is a method and/or apparatus for adjusting the sample time and order associated with a digital correction system for maximizing output power and minimizing power stage delay sensitivity of a switching power stage. In certain embodiments, the sample point of an ADC may be changed as a function of the duty ratio of the PWM signal thus allowing higher performance and use of less expensive power stage components. In addition, adjustment of the order of an integrating error amplifier in the system permits operation of the power stage with an output being permitted to saturate up to the power supply rails, thus increasing a power output of the power stage.